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SIMULATION OF NEURAL NETWORKS BY OPTICAL-PHOTOGRAPHIC METHODS

by

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A method of using photographic film and pin-hole optical wiring is proposed here that seems particularly suited for simulating an electronic data processing machine having many elements operating in parallel. The maximum size of this machine would seem to be about 10,000 neural elements with a storage capability of 100 levels in each element. A number of sequential photographic exposures and developments would be required to adjust the internal states of the simulator for each input pattern that has to be "learned", and the total time involved in film processing would be approximately thirty minutes. One prime advantage of this optical simulation method over its electronic counterpart would be the ability to progressively change the internal wiring toward an optimum configuration in a self-converging manner.

Each function of an electronic machine is simulated optically and photographically, the optical analogue represented on photographic film could be used to construct an electronic machine of equivalent design. This method of data processing is based upon the following analogies between electronic and photographic functions:

Electronic Function	Photographic Method
Amplification	High sensitivity film emulsion
Threshold or Gating	High contrast film
Wiring	Optical paths in air through transparent holes in high contrast film
Memory	Variable density of developed film
Negation	Reversal printing of film
Adder	Summation of various light paths and intensities on sensitive film
Multiplier	Transmission of light intensity X through film of density Y

EXAMPLE OF SIMULATED FUNCTIONS

Using a set of typical functions assumed useful in a neural network, an example will be given showing how this function may be simulated photo-optically; next, an optical method will be shown that is capable of interconnecting a number of these elements; and finally, a photo-optical method will be described that is capable of modifying the interconnections as a function of some internal state of the machine.

Assume that many elements are treated simultaneously, and that the following function represents one element in a particular network which is to be simulated:

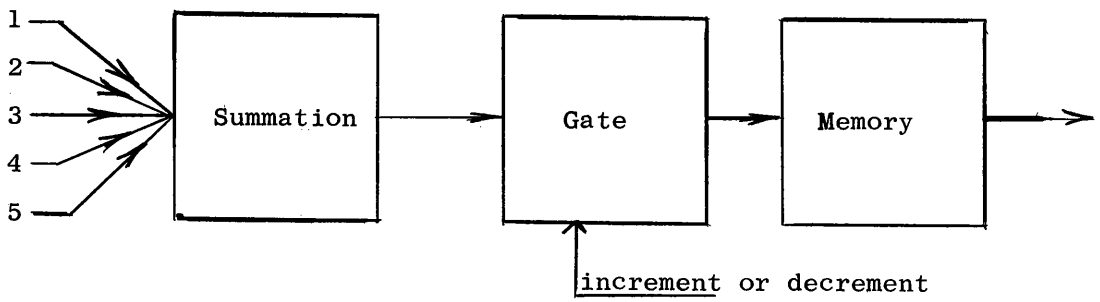

Fig. 1

The functional operations desired (Fig. 1) are a number of inputs be summed, and if their sum exceeds some arbitrary threshold, the gate opens, permitting non-destructive read-out of a stored value in the analog memory. This unit is then defined as active. The open gate of active units also permits subsequent incrementing or decrementing of the value in the memory.

The steps needed to simulate above functions are: 1) Expose a high contrast film with the various overlapping input light beams, then develop so as to produce a black spot if the combined lights rays are intense enough; 2) Contact print the plate of Step 1 on another high contrast plate to improve the clipping and to give a clear spot on a dark background. This plate is called the gate plate and its selected clear spots represent active elements; 3) If non-destructive read-out is the next desired function, then diffuse light is permitted to pass through the gate plate in Step 2 superimposed on a previously obtained memory plate. The memory plate has a multiplicity of spots of varying density, the density representing the stored value. The gate plate thus selects for read-out through the memory plate only those elements which have been made active. The light output from the various elements of the selected memory spots can then be grouped in some desired manner by use of an optical wiring plate and can subsequently be summed and measured in intensity; 4) If the required function is to change only the values of active units in the memory plate, representing an up-dating of stored information, the following procedure is effected: to preserve old information which is not to be altered, a reversal is made of the gate plate yielding opaque spots for active units and transparent spots for all others; a reversal

is also made of the old memory plate; a contact print is now made with light permitted to pass through both the gate and memory plate reversals to the new plate. The new plate thus far has preserved the values of only those elements which were not active, leaving unexposed those spots representing active elements. Before developing, a second exposure is made to reintroduce the active element values, either incremented or decremented in value; this is done by exposing through the original gate plate (Step 2), the old memory plate and a previously prepared increment or decrement plate. The new memory plate is now developed with both sets of latent images.

The above steps illustrated just one of the methods that will produce the desired result. A great deal of freedom in photographic plate exposing and developing is possible. For instance, if it is desired to "decay" the memory, the photographic plate may be slightly overexposed then developed at a gamma lower than one. This has the effect of a fixed percentage decay of all values toward an arbitrary zero at some mid-density value for the film.

This photo-optical simulation method offers a convenient display for an operator to follow the progress of the internal states of the machine. A plate can be developed which shows only the changes from one step in the "learning" to another, making the machine's progress easier to follow. This is done by simultaneously printing a new memory plate positive and an old memory plate negative so that only changes appear in the finished plate.

OPTICAL WIRING

When a group of neural elements are to be connected, an operator may then specify which light paths through transparent holes in an otherwise opaque film will serve to couple the units. An example of this may be shown in the coupling of an input pattern to various neural elements.

In Figure 2 a diffuse uniform source of light passes through the input pattern plate to produce any desired intensity at the input mosaic. The mosaic film is a uniform array of small holes. The wiring pattern plate is a high contrast film with small transparent holes at selected locations. Any desired change in wiring merely requires a new wiring pattern plate.

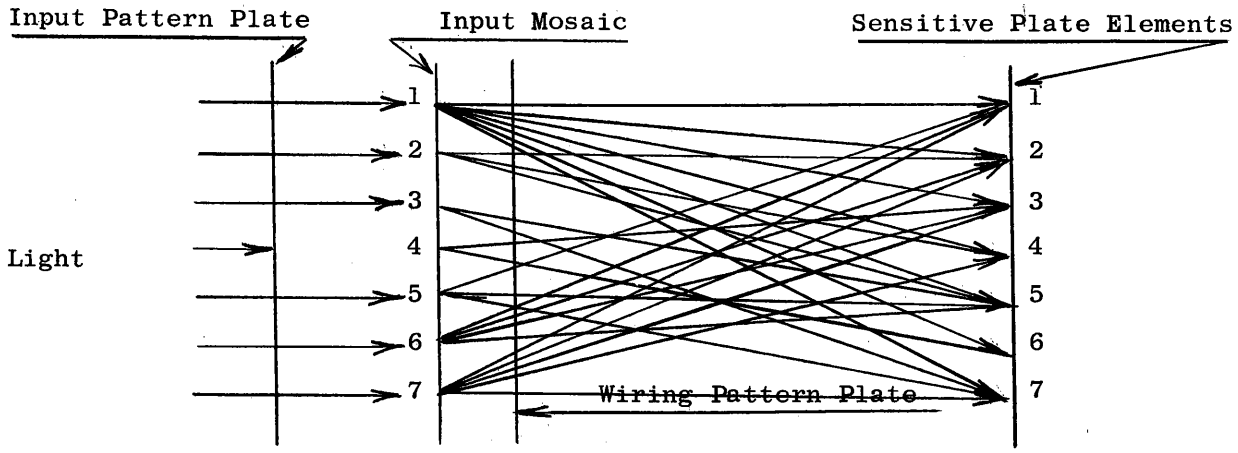

Fig. 2

In this example the input pattern illuminates all mosaic elements except #4.

The connections established between the input mosaic elements and the sensitive plate elements are:

Input Mosaic Element	Sensitive Plate Element
1	1,2,3,4,5,6,7
2	2,4,5
3	5,7
4	3,6
5	1,5,7
6	1,2,3,5
7	1,2,3,4,7

Under the conditions given, the values of the sensitive plate elements would be:

Element	Value
1	4
2	4
3	3
4	3
5	5
6	1
7	4

Any position on the input mosaic may be connected to any or all of the sensitive plate elements and the value of illumination depends upon the number and intensities of the various light paths. Since light values accumulated by the sensitive plate cannot be subtracted, negative values from the input mosaic are obtained by developing a sensitive plate from a negative wiring pattern, and using this as an attenuator in front of the sensitive plate during the positive wiring pattern exposure.

SELF-OPTIMIZATION OF OPTICAL WIRING

The term, self-optimization of wiring, as used here, indicates that improvements in the wiring of a machine can be made without an operator attending to the detailed wiring paths themselves, but rather to a gross process which results in wiring improvements.

If the wiring of the machine is to be self-optimizing, then some internal state must be made to indicate an improved configuration. For our example let us suppose that the low value of a memory element serves as an indication of poor connections to that cell, and in this example we shall call for a new set of connections to random points in the input mosaic.

This method of wiring optimization is composed of the following major steps: 1) Determination of inadequate wiring paths, 2) Removal of inadequate wiring paths, 3) Selection of new connection paths, and 4) Addition of new paths to previously correct paths.

To satisfy Step 1, we may take a gate plate that has been produced from the memory plate such as to give transparent spots wherever suitably low or inactive memory values are found. The low value found in element #6 of Figure 2 may illustrate this.

In order to satisfy Step 2, the wires from input mosaic #1 and #4 must be removed. This is a two-step process in which the incorrect paths are first identified; then a mask is made that will fit over the input mosaic to blot out these incorrect paths while all of the correct paths are being passed on to a new plate. The incorrect paths are identified by using the optical projection method shown in Figure 3.

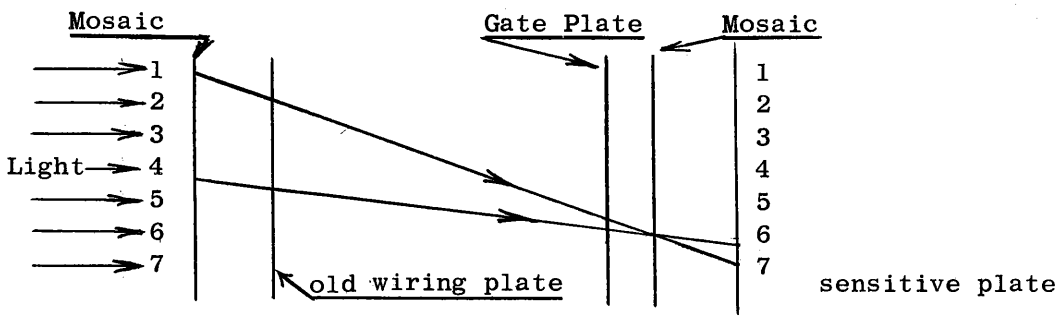

Fig.3

The gate plate is used to select which area of the memory plate is inactive, and the mosaic element associated with it is used to reduce the size of the light beam falling on the sensitive plate, and to locate the input elements from which the light comes. The sensitive plate obtained above must be developed and a high contrast negative made from it. This negative plate, having small transparent spots in it, positioned where the incorrect paths are, is now projected back as shown in Fig. 4, to a new film so as to produce black spots that will be used later to blot out the incorrect paths when the old wiring pattern is copied on a new film.

The mosaic element near the sensitive film in Fig. 4 is used to reduce the light spot to the desired size.

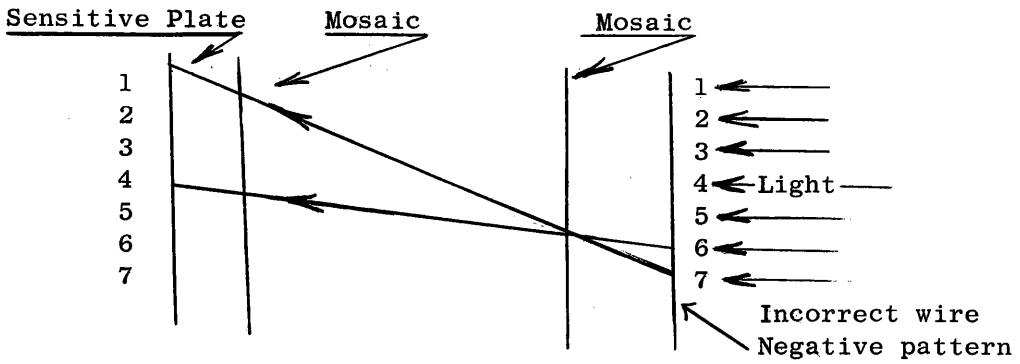

Fig. 4

The selection of a new group of random connections to satisfy Step 3 may be done by generating a wiring pattern plate with somewhat larger outside dimensions than required and having groups of holes associated with each mosaic element that will be randomly positioned. This film is used whenever new wires must be added, and its two lateral positions are randomly set each time, thus generating very slight correlation between the various wiring changes.

To complete Step 4, it is necessary to make a contact print of the old wiring pattern through the connection removal pattern generated in Step 2 and then the new connections are added by projection of the random hole positions in Step 3 through a gate plate in an optical system similar to Fig. 4, the random plate substituting for the incorrect wire negative pattern. Since all operations on a single plane or film are carried out in parallel, the number of elements in the machine does not affect the processing time.

PROBLEMS AND LIMITATIONS

The following problems have been noted for this simulation method and a tentative solution for each is mentioned:

1) Uniformity of lighting: The uniformity of the light source must be corrected to within 1% for 100 levels of storage. This compensation can be done by developing a negative film image of the source and placing it over the source so as to remove highlights. The changes in light intensity on the sensitive film from the various wiring paths vary with angle of illumination and path length. This can be compensated with a variable density film placed over the wiring pattern plate so as to give a few percent less light to the normal angle or short light paths.

2) Scattered and stray light effects: Multiple reflections in the support materials used for optical wiring become troublesome for glass plates, but are avoided with film materials. The illuminating aperture angle must be reduced to the minimum required by the optical wiring or reflections from container walls become troublesome. Adequate blackening of walls also reduces this problem. Diffraction effects have been avoided thus far by using large pin holes for wiring paths.

3) Mechanical requirements: Mechanical registration of various adjacent elements such as a mosaic element and a wiring pattern plate must be maintained to within a few thousands of an inch in three dimensions to prevent adjacent channel interference and to maintain unity magnification for the system. A honeycomb type of vacuum frame is presently used and has been found adequate.

4) Materials and processes: A high degree of quality control on the photographic materials used for the gating and memory functions is desirable. In order to maintain proper process control, a gray scale must be processed along with each film used for gating and memory and be checked upon completion of the process so as to prevent

accumulative error. Dust particles must be very carefully controlled whenever a wiring plate is used or made although gates and memory elements can average out the effects of small quantities of dust because of their extended areas.

Using state-of-the-art photographic methods and materials one hundred levels of storage and gating have been obtained under laboratory conditions involving very few samples of material. A wiring plate and mosaic for 1000 neural elements has been tested in which the cross talk between adjacent elements is less than 300 to 1. A six-inch by six-inch film is used throughout for mosaic, wiring, gating, and memory. The wiring plate hole size is 0.005 inch diameter and the gate and memory spot size is 0.2 inch diameter maximum. A simulator for 10,000 neural elements would use a film size of 18 x 18 inches.